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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SUN, XIUQIN	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/930,971	CHEN ET AL.
	Examiner	Art Unit
	Xiuqin Sun	2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higuchi (U.S. Pat. No. 5790400) in view of Nara et al. (U.S. Pat. No. 6388747 B2) and Ogata et al. (U.S. Pat. No. 6281962 B1).

Higuchi teaches an apparatus, system and method of object inspection (see abstract), comprising: a process executor requesting a plurality of objects to be inspected at a first sampling rate and receiving a plurality of inspection results (col. 1, lines 62-67; col. 2, lines 1-4; col. 2, lines 33-58; col. 5, lines 22-38; and col. 8, lines 58-61); a data processor analyzing the inspection results to determine a second sampling rate (col. 7, lines 50-67); a device storing the second sampling rate (col. 2, lines 15-22; col. 3, lines 19-25 and col. 7, lines 50-67); a controller receiving said second sampling rate from the storage device and changing said first sampling rate of the inspection requested by the process controller to said second sampling rate (col. 7, lines 50-67and col. 2, lines 15-22); an input device connected to the storage device for inputting of user-defined data (col. 1, lines 62-67; col. 2, lines 1-4 and col. 2, lines 33-58).

Higuchi does not mention explicitly: the objects to be inspected is a plurality of semi-manufactured products processed by a manufacturing equipment; an input device connected to the storage device for inputting of a user-defined sampling rate; a display connected to the storage device, displaying the first and the second sampling rates; and said apparatus, system and method is used for dynamically monitoring stability of manufacturing equipment.

Nara et al. disclose a inspection method, apparatus and system for circuit pattern, and teach: a process executor for requesting a plurality of semi-manufactured products processed by a semiconductor manufacturing equipment to be inspected at a given sampling rate and receiving a plurality of inspection results (see Figs. 2 and 4; col. 8, lines 45-67; col. 9, lines 1-7, lines 37-50; col. 10, lines 62-67; col. 11, lines 1-17; col. 28, lines 58-67 and col. 42, lines 14-24). Nara et al. further teach: an input device connected to the storage device for inputting of a user-defined sampling rate (col. 28, lines 31-41 and lines 58-63); and a display connected to the storage device, displaying the sampling rate for the inspection process (see Fig. 25 and col. 28, lines 27-41).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teachings of Nara process executor, sampling rate input means and the display means in the Higuchi system and method in order to automatically execute the parameter setting and data process in parallel with the inspecting operation (Nara, col. 2, lines 53-65), and display the output in a user-friendly GUI format (Fig. 25).

Ogata et al. disclose an inspection equipment and method for detecting defects in a wafer in a coating and developing system. Ogata et al. teach: dynamically monitoring and controlling stability of the manufacturing equipment and adjusting inspection frequency according to inspection results obtained during the monitoring process (col. 5, lines 8-54 and col. 7, lines 45-60).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the teachings of Ogata et al. in the Higuchi system and method in order to provide a better product inspection technique that is capable of dynamically monitoring the stability of a semiconductor manufacturing equipment and providing feedback control of the manufacturing process (Ogata et al., see Abstract).

3. Claims 4-5 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higuchi in view of Nara et al. and Ogata et al., as applied to claim 1 above, and further in view of Li (U.S. Pat. No. 6276997).

Higuchi, Nara et al. and Ogata et al. teach a method and apparatus that includes the subject matter discussed above except that: a semiconductor manufacturing process that is capable of etching the semi-manufactured products such as a wafer and a technique for forming an oxide layer on the semi-manufactured products.

Nara et al. further teach a semiconductor manufacturing process that is capable of etching the semi-manufactured products such as a wafer (see Fig. 5 and col. 11, lines 43-67).

Li discloses a method and system and teaches: a technique for forming an oxide layer on the semi-manufactured products (col. 2, lines 12-21).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the teaching of Nara semiconductor manufacturing process and Li oxide layer formation technique in the combination of Higuchi and Ogata et al. in order to apply the stability monitoring to semiconductor manufacturing process such as etching a semiconductor wafer (Nara, col. 1, lines 29-41; and Li, col. 2, lines 12-21).

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higuchi in view of Nara et al. and Ogata et al., as applied to claim 1 above, and further in view of Sandoval (U.S. Pat. No. 6345259).

Higuchi, Nara et al. and Ogata et al. teach a method and apparatus that includes the subject matter discussed above except that: the process executor is a Manufacturing Executive System (MES).

Sandoval teaches a Manufacturing Executive System (MES) that serves as a process executor used in a computer integrated manufacturing environment (col. 4, lines 27-33; col. 11, lines 6-16 and lines 29-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the teaching of Sandoval MES in the combination of Higuchi, Nara and Ogata et al. in order to provides an automated, multi-directional computer integrated manufacturing system and to enable computer integrated manufacturing (Sandoval, col. 4, lines 25-36).

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higuchi in view of Nara et al. and Ogata et al., as applied to claim 1 above, and further in view of Webster (U.S. Pat. No. 5505090).

Higuchi, Nara et al. and Ogata et al. teach a method and system that includes the subject matter discussed above except that: the inspection of the semi-manufacturing products is non-destructive.

Webster teaches a method and apparatus for non-destructive inspection of composite materials such as the semi-manufacturing products (see abstract) by sampling the products at a given sampling rate (col. 9, lines 32-50).

It would have been obvious to include the teaching of Webster technique for non-destructive inspection of semi-manufacturing products in the combination of Higuchi, Nara and Ogata et al. in order to provide a practical technique non-destructively locating faults in composite structures which is suitable not only for in-plant non-destructive evaluation but for field use as well (Webster, col. 1, lines 32-42).

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higuchi in view of Nara et al. and Ogata et al., as applied to claim 1 above, and further in view of Schmolke et al. (U.S. Pat. No. 6333785).

Higuchi, Nara et al. and Ogata et al. teach a method and system that includes the subject matter discussed above except that: using a thickness of an oxide layer as a standard for inspection.

Schmolke et al. teach a method in which the thickness of an oxide layer is used as the standard in inspecting a smooth surface of semiconductor wafers (col. 3, lines 45-60 and col.4, lines 1-5).

It would have been obvious to include the teaching of Schmolke inspection of thickness of an oxide layer in the combination of Higuchi, Nara and Ogata et al. in order to provide a system for quality inspection of a semiconductor object that uses the thickness of an oxide layer as a standard for inspection (Schmolke, col. 3, lines 45-59 and col. 4, lines 1-5).

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higuchi in view of Nara et al. and Ogata et al., and further in view of Charles (U.S. Pat. No. 6335559).

Higuchi, Nara et al. and Ogata et al. teach a method and system that includes the subject matter discussed above except that: using an etching depth as a standard for inspection.

Charles teaches a method and device that can monitor the operation of etching a semiconductor wafer by inspecting the etching depth (col. 7, lines 36-53).

It would have been obvious to include the teaching of Charles inspection of etching depth in the combination of Higuchi, Nara and Ogata et al. in order to conduct quality inspection of a semiconductor object by examining the etching depth as a standard for inspection (Charles, col.7, lines 36-53).

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable Higuchi in view of Nara et al. and Ogata et al., and further in view of Hinkle (U.S. Pat. No. 6190313).

Higuchi, Nara et al. and Ogata et al. teach a method and system that includes the subject matter discussed above except that: the data processor is an SPC analyzing software application.

Hinkle teaches an Statistical Process Control (SPC) analyzing software application used as a data processor in processing and analyzing the data in question (see abstract; col. 2, lines 59-61 and col. 3, lines 49-61)

It would have been obvious to include the teaching of the Hinkle SPC analyzer in the combination of Higuchi, Nara and Ogata et al. in order to perform a SPC analysis on the indexed data records (Hinkle, abstract).

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higuchi. in view of Nara et al. and Ogata et al., and further in view of Juszkiewicz et al. (U.S. Pat. No. 6353169).

Higuchi, Nara et al. and Ogata et al. teach an apparatus and method that includes the subject matter discussed above except that: said controller is a server.

Juszkiewicz et al. teach a controller that has the capability of converting sampling rates (col. 13, lines 24-38), and the controller is of the functionality of a server (col. 3, lines 62-65).

It would have been obvious to include the teaching of Juszkiewicz et al. server type of controller in the combination of Higuchi, Nara and Ogata et al. in order to

dynamically configure the system and control the operation of the system (Juszkiewicz, col. 3, lines 62-67 and col.4, lines 43-45).

Response to Arguments

10. Applicants' arguments received 02/27/2004 with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Claims 1-13 are rejected as new art (U.S. Pat. No. 6281962 B1 to Ogata et al.) has been found to teach the limitation of monitoring stability of manufacturing equipment and adjusting inspection frequency according to inspection results obtained during the monitoring process. In particular, it is deemed that the combination of Higuchi, Nara et al. and Ogata et al. patents teaches or suggests an inspection system capable of monitoring run-to-run variability in semiconductor manufacturing. Detailed response is given in section 2 set forth above in this Office Action.

Prior Art Citations

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1) Naruoka (U.S. Pat. No. 6300147) disclose a method and system of inspecting semiconductor substrate.

2) Takagi et al. (U.S. Pub. No. 20010020194) disclose a method and system for manufacturing semiconductor devices, and method and system for inspecting semiconductor devices.

3) Morioka et al. (U.S. Pat. No. 5274434) disclose a method and apparatus for inspecting foreign particles on real time basis in semiconductor mass production line.

Contact Information

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Xiuqin Sun whose telephone number is (571)272-2280. The examiner can normally be reached on 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571)272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Xiuqin Sun
Examiner
Art Unit 2863

John Barlow
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Technology Center 2800

XS
September 17, 2004